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KEY=FOR - ALVAREZ FRIEDMAN

3D IC AND RF SIPS: ADVANCED STACKING AND PLANAR SOLUTIONS FOR 5G MOBILITY

John Wiley & Sons An interdisciplinary guide to enabling technologies for 3D ICs and 5G mobility, covering packaging, design to product life and reliability assessments Features an interdisciplinary approach to the enabling technologies and hardware for 3D ICs and 5G mobility Presents statistical treatments and examples with tools that are easily accessible, such as Microsoft’s Excel and Minitab Fundamental design topics such as electromagnetic design for logic and RF/passives centric circuits are explained in detail Provides chapter-wise review questions and powerpoint slides as teaching tools

ADVANCED PACKAGING

Advanced Packaging serves the semiconductor packaging, assembly and test industry. Strategically focused on emerging and leading-edge methods for manufacturing and use of advanced packages.

SEMICONDUCTOR ADVANCED PACKAGING

Springer Nature The book focuses on the design, materials, process, fabrication, and reliability of advanced semiconductor packaging components and systems. Both principles and engineering practice have been addressed, with more weight placed on engineering practice. This is achieved by providing in-depth study on a number of major topics such as system-in-package, fan-in wafer/panel-level chip-scale packages, fan-out wafer/panel-level packaging, 2D, 2.1D, 2.3D, 2.5D, and 3D IC integration, chiplets packaging, chip-to-wafer bonding, wafer-to-wafer bonding, hybrid bonding, and dielectric materials for high speed and frequency. The book can benefit researchers, engineers, and graduate students in fields of electrical engineering, mechanical engineering, materials sciences, and industry engineering, etc.

ADVANCED PACKAGING

Advanced Packaging serves the semiconductor packaging, assembly and test industry. Strategically focused on emerging and leading-edge methods for manufacturing and use of advanced packages.

3D IC STACKING TECHNOLOGY

McGraw Hill Professional The latest advances in three-dimensional integrated circuit stacking technology With a focus on industrial applications, 3D IC Stacking Technology offers comprehensive coverage of design, test, and fabrication processing methods for three-dimensional device integration. Each chapter in this authoritative guide is written by industry experts and details a separate fabrication step. Future industry applications and cutting-edge design potential are also discussed. This is an essential resource for semiconductor engineers and portable device designers. 3D IC Stacking Technology covers: High density through silicon stacking (TSS) technology Practical design ecosystem for heterogeneous 3D IC products Design automation and TCAD tool solutions for through silicon via (TSV)-based 3D IC stack Process integration for TSV manufacturing High-aspect-ratio silicon etch for TSV Dielectric deposition for TSV Barrier and seed deposition Copper electrodeposition for TSV Chemical mechanical polishing for TSV applications Temporary and permanent bonding Assembly and test aspects of TSV technology

ADVANCED FLIP CHIP PACKAGING

Springer Science & Business Media Advanced Flip Chip Packaging presents past, present and future advances and trends in areas such as substrate technology, material development, and assembly processes. Flip chip packaging is now in widespread use in computing, communications, consumer and automotive electronics, and the demand for flip chip technology is continuing to grow in order to meet the need for products that offer better performance, are smaller, and are environmentally sustainable.

SYSTEMS-LEVEL PACKAGING FOR MILLIMETER-WAVE TRANSCEIVERS

Springer This book provides a system-level approach to making packaging decisions for millimeter-wave transceivers. In electronics, the packaging forms a bridge between the integrated circuit or individual device and the rest of the electronic system, encompassing all technologies between the two. To be able to make well-founded packaging decisions, researchers need to understand a broad range of aspects, including: concepts of transmission bands, antennas and propagation, integrated and discrete package substrates, materials and technologies, interconnects, passive and active components, as well as the advantages and disadvantages of various packages and packaging approaches, and package-level modeling and simulation. Packaging also needs to be considered in terms of system-level testing, as well as associated testing and production costs, and reducing costs. This peer-reviewed work contributes to the extant scholarly literature by addressing the aforementioned concepts and applying them to the context of the millimeter-wave regime and the unique opportunities that this transmission approach offers.

SIP SYSTEM-IN-PACKAGE DESIGN AND SIMULATION

MENTOR EE FLOW ADVANCED DESIGN GUIDE

John Wiley & Sons Cover -- Title Page -- Copyright -- Contents -- About the Author -- Preface -- Chapter 1 SiP Design and Simulation Platform -- 1.1 From package to SiP -- 1.2 The development of mentor SiP design technology -- 1.3 The mentor SiP design and simulation platform -- 1.3.1 SiP platform introduction -- 1.3.2 Schematic input -- 1.3.3 Concurrent system design -- 1.3.4 SiP board design -- 1.3.5 Signal integrity and power integrity simulation -- 1.3.6 Thermal analysis -- 1.3.7 The advantages of the mentor SiP design and simulation platform -- 1.3.7.1 Characteristics of mentor SiP design and simulation platform -- 1.3.7.2 Design areas of mentor SiP design and simulation platform -- 1.4 The introduction of the finished project -- Chapter 2 Introduction to Package -- 2.1 Definition and function of package -- 2.2 Development of packaging technology -- 2.3 SiP and Related Technologies -- 2.3.1 The appearance of SiP technology -- 2.3.2 SoC and SiP -- 2.3.3 SiP-related technologies -- 2.4 The development of the package market -- 2.5 Package manufacturers -- 2.5.1 Traditional package manufacturers -- 2.5.2 New SiP manufacturers in different areas -- 2.6 Bare chip suppliers -- Chapter 3 The SiP Production Process -- 3.1 BGA: The mainstream SiP package form -- 3.2 The SiP package production process -- 3.3 Three key elements of SiP -- Chapter 4 New Package Technologies -- 4.1 TSV (Through Silicon Via) technology -- 4.1.1 TSV introduction -- 4.1.2 TSV technical characteristics -- 4.1.3 TSV application and prospects -- 4.2 Integrated passive device (IPD) technology -- 4.2.1 IPD introduction -- 4.2.2 The advantages of IPD -- 4.3 Package on package (PoP) technology -- 4.3.1 The limitations of 3D SiP -- 4.3.2 The application of PoP -- 4.3.3 The emphasis in PoP design -- 4.4 Apple A8 processor - an example of a PoP product -- Chapter 5 SiP Design and Simulation Flow

HETEROGENEOUS INTEGRATIONS

Springer Heterogeneous integration uses packaging technology to integrate dissimilar chips, LED, MEMS, VCSEL, etc. from different fabless houses and with different functions and wafer sizes into a single system or subsystem. How are these dissimilar chips and optical components supposed to talk to each other? The answer is redistribution layers (RDLs). This book addresses the fabrication of RDLs for heterogeneous integrations, and especially focuses on RDLs on: A) organic substrates, B) silicon substrates (through-silicon via (TSV)-interposers), C) silicon substrates (bridges), D) fan-out substrates, and E) ASIC, memory, LED, MEMS, and VCSEL systems. The book offers a valuable asset for researchers, engineers, and graduate students in the fields of semiconductor packaging, materials sciences, mechanical engineering, electronic engineering, telecommunications, networking, etc.

CHINA SEMICONDUCTOR TECHNOLOGY INTERNATIONAL CONFERENCE 2010 (CSTIC 2010)

The Electrochemical Society Our mission is to provide a forum for world experts to discuss technologies, address the growing needs associated with silicon technology, and exchange their discoveries and solutions for current issues of high interest. We encourage collaboration, open discussion, and critical reviews at this conference. Furthermore, we hope that this conference will also provide collaborative opportunities for those who are interested in the semiconductor industry in Asia, particularly in China.

MILLIMETER-WAVE INTEGRATED CIRCUITS

METHODOLOGIES FOR RESEARCH, DESIGN AND INNOVATION

Springer Nature This peer-reviewed book explores the methodologies that are used for effective research, design and innovation in the vast field of millimeter-wave circuits, and describes how these have to be modified to fit the uniqueness of high-frequency nanoelectronics design. Each chapter focuses on a specific research challenge related to either small form factors or higher operating frequencies. The book first examines nanodevice scaling and the emerging electronic design automation tools that can be used in millimeter-wave research, as well as the singular challenges of combining deep-submicron and millimeter-wave design. It also demonstrates the importance of considering, in the millimeter-wave context, system-level design leading to differing packaging options. Further, it presents integrated circuit design methodologies for all major transceiver blocks typically employed at millimeter-wave frequencies, as these methodologies are normally fundamentally different from the traditional design methodologies used in analogue and lower-frequency electronics. Lastly, the book discusses the methodologies of millimeter-wave research and design for extreme or harsh environments, rebooting electronics, the additional opportunities for terahertz research, and the main differences between the approaches taken in millimeter-wave research and terahertz research.

THREE-DIMENSIONAL INTEGRATED CIRCUIT DESIGN

Newnes Three-Dimensional Integrated Circuit Design, Second Eition, expands the original with more than twice as much new content, adding the latest developments in circuit models, temperature considerations, power management, memory issues, and heterogeneous integration. 3-D IC experts Pavlidis, Savidis, and Friedman cover the full product development cycle throughout the book, emphasizing not only physical design, but also algorithms and system-level considerations to increase speed while conserving energy. A handy, comprehensive reference or a practical design guide, this book provides effective solutions to specific challenging problems concerning the design of three-dimensional integrated circuits. Expanded with new chapters and updates throughout based on the latest research in 3-D integration: Manufacturing techniques for 3-D ICs with TSVs Electrical modeling and closed-form expressions of through silicon vias Substrate noise coupling in heterogeneous 3-D ICs Design of 3-D ICs with inductive links Synchronization in 3-D ICs Variation effects on 3-D ICs Correlation of WID variations for intra-tier buffers and wires Offers practical guidance on designing 3-D heterogeneous systems Provides power delivery of 3-D ICs Demonstrates the use of 3-D ICs within heterogeneous systems that include a variety of materials, devices, processors, GPU-CPU integration, and more Provides experimental case studies in power delivery, synchronization, and thermal characterization

ISTFA 2014

CONFERENCE PROCEEDINGS FROM THE 40TH INTERNATIONAL SYMPOSIUM FOR TESTING AND FAILURE ANALYSIS

ASM International This volume features the latest research and practical data from the premier event for the microelectronics failure analysis community. The papers address the symposium's theme, Exploring the Many Facets of Failure Analysis.

ENABLING TECHNOLOGIES FOR 3-D INTEGRATION: VOLUME 970

Materials Research Society An emerging technology or device architecture called 3-D IC integration is based on the system performance gains that can be achieved by stacking and vertically interconnecting distinct device chips. The 3-D concept of replacing long 2-D interconnects with shorter vertical (3-D) interconnects has the potential to alleviate the well-known interconnect (RC) delay problem facing the semiconductor industry. Additional benefits of the 3-D concept for the IC maker include reduced die size and the ability to use distinct technologies (analog, logic, RF, etc...) on separate vertically interconnected layers. The 3-D concept, therefore, allows the integration of otherwise incompatible technologies, and offers significant advantages in performance, functionality, and form factor. Topics in this book include: fabrication of 3-D ICs; modeling, simulation and scaling of 3-D integrated devices; applications of 3-D integration; through wafer interconnects for 3-D packaging and interposer applications; bonding technology for 3-D integration; and enabling processes for 3-D integration.

MICROSYSTEM BASED ON SIP TECHNOLOGY

Springer This book is a comprehensive SiP design guide book. It is divided into three parts: concept and technology, design and simulation, project and case, for a total of 30 chapters. In Part one, the author proposes some new original concepts and thoughts, such as Function Density Law,Si3P and 4D integration. Part one also covers the latest technology of SiP and Advanced Packaging. Part two covers the latest SiP and Advanced Packaging design and simulation technologies, such as wire bonding, multi-step cavity, chip stacking, 2.5D TSV, 3D TSV, RDL, Fan- In, Fan-Out, Flip Chip, Embedded Passive, Embedded Chip, RF design, Rigid-Flex design, 4D SiP design, Multi-layout project and Team design, as well as SI, PI, thermal simulation, electrical verification and physical verification. Based on a

real design case, part three introduces the design, simulation and implementation methods of different types of SiP, which has a -important reference significance for the research and development of SiP projects. This book comprehensively and deeply expounds the latest development, design ideas and design methods of contemporary SiP technology from three aspects: concept and technology, design and simulation, project and case. Through the detailed introduction of new concepts, design methods, actual projects and cases, this book describes the whole process of SiP products from the beginning of conception to the final realization and makes readers benefit from it.

RELIABILITY OF ROHS-COMPLIANT 2D AND 3D IC INTERCONNECTS

McGraw Hill Professional Proven 2D and 3D IC lead-free interconnect reliability techniques Reliability of RoHS-Compliant 2D and 3D IC Interconnects offers tested solutions to reliability problems in lead-free interconnects for PCB assembly, conventional IC packaging, 3D IC packaging, and 3D IC integration. This authoritative guide presents the latest cutting-edge reliability methods and data for electronic manufacturing services (EMS) on second-level interconnects, packaging assembly on first-level interconnects, and 3D IC integration on microbumps and through-silicon-via (TSV) interposers. Design reliable 2D and 3D IC interconnects in RoHS-compliant projects using the detailed information in this practical resource. Covers reliability of: 2D and 3D IC lead-free interconnects CCGA, PBGA, WLP, PQFP, flip-chip, lead-free SAC solder joints Lead-free (SACX) solder joints Low-temperature lead-free (SnBiAg) solder joints Solder joints with voids, high strain rate, and high ramp rate VCSEL and LED lead-free interconnects 3D LED and 3D MEMS with TSVs Chip-to-wafer (C2W) bonding and lead-free interconnects Wafer-to-wafer (W2W) bonding and lead-free interconnects 3D IC chip stacking with low-temperature bonding TSV interposers and lead-free interconnects Electromigration of lead-free microbumps for 3D IC integration

ADVANCED METALLIZATION CONFERENCE 2002 (AMC 2002)

PROCEEDINGS OF THE CONFERENCE HELD OCTOBER 1-3, 2002, IN SAN DIEGO, CALIFORNIA, U.S.A., AND OCTOBER 29-30, 2002, UNIVERSITY OF TOKYO, JAPAN

SYSTEM ON PACKAGE

MINIATURIZATION OF THE ENTIRE SYSTEM

McGraw Hill Professional System-on-Package (SOP) is an emerging microelectronic technology that places an entire system on a single chip-size package. Where “systems” used to be bulky boxes housing hundreds of components, SOP saves interconnection time and heat generation by keep a full system with computing, communications, and consumer functions all in a single chip. Written by the Georgia Tech developers of the technology, this book explains the basic parameters, design functions, and manufacturing issues, showing electronic designers how this radical new packaging technology can be used to solve pressing electronics design challenges.

IEICE TRANSACTIONS ON ELECTRONICS

先進微電子3D-IC構裝

五南圖書出版股份有限公司在構裝技術尚未完全進入3D TSV量產之前，FOWLP為目前最具發展潛力的新興技術。此技術起源於英飛凌(Infineon)在2001年所提出之嵌入式晶片扇出專利，後續於2006年發表技術文件後，環氧樹脂化合物(EMC)之嵌入式晶片，也稱作扇出型晶圓級構裝(FOWLP)，先後被應用於各種元件上，例如：基頻(Baseband)、射頻(RF)收發器和電源管理IC(PMIC)等。其中著名公司包括英飛凌、英特爾(Intel)、Marvell、展訊(Spreadtrum)、三星(Samsung)、LG、華為(Huawei)、摩托羅拉(Motorola)和諾基亞(Nokia)等，許多半導體外包構裝測試服務(OSATS)和代工廠(Foundry)，亦開發自己的嵌入式FOWLP，預測在未來幾年，FOWLP市場將有爆炸性之成長。有鑑於此，第三版特別新增第13章扇出型晶圓級(Fan-out WLP)構裝之基本製程與發展概況、第14章嵌入式扇出型晶圓級或面板級構裝(Embedded Fan-out WLP/PLP)技術，以及第15章 3D-IC導線連接技術之發展狀況。在最新第四版特別增加：第16章扇出型面版級封裝技術的演進，第17章3D-IC異質整合構裝技術。本書適合於有志從事半導體製程研發、生產和應用之工程技術人員，以及產品推廣與技術行銷人員閱讀，也可作為電子、電機、光電、材料、化工、機械、應用物理及應用化學等相關系所學習之參考用書。

THROUGH-SILICON VIAS FOR 3D INTEGRATION

McGraw Hill Professional A comprehensive guide to TSV and other enabling technologies for 3D integration Written by an expert with more than 30 years of experience in the electronics industry, Through-Silicon Vias for 3D Integration provides cutting-edge information on TSV, wafer thinning, thin-wafer handling, microbumping and assembly, and thermal management technologies. Applications to highperformance, high-density, low-power-consumption, wide-bandwidth, and small-form-factor electronic products are discussed. This book offers a timely summary of progress in all aspects of this fascinating field for professionals active in 3D integration research and development, those who wish to master 3D integration problem-solving methods, and anyone in need of a low-power, wide-bandwidth design and high-yield manufacturing process for interconnect systems. Coverage includes: Nanotechnology and 3D integration for the semiconductor industry TSV etching, dielectric-, barrier-, and seed-layer deposition, Cu plating, CMP, and Cu revealing TSVs: mechanical, thermal, and electrical behaviors Thin-wafer strength measurement Wafer thinning and thin-wafer handling Microbumping,

assembly, and reliability Microbump electromigration Transient liquid-phase bonding: C2C, C2W, and W2W 2.5D IC integration with interposers 3D IC integration with interposers Thermal management of 3D IC integration 3D IC packaging

HANDBOOK OF 3D INTEGRATION, VOLUME 4

DESIGN, TEST, AND THERMAL MANAGEMENT

John Wiley & Sons This fourth volume of the landmark handbook focuses on the design, testing, and thermal management of 3D-integrated circuits, both from a technological and materials science perspective. Edited and authored by key contributors from top research institutions and high-tech companies, the first part of the book provides an overview of the latest developments in 3D chip design, including challenges and opportunities. The second part focuses on the test methods used to assess the quality and reliability of the 3D-integrated circuits, while the third and final part deals with thermal management and advanced cooling technologies and their integration. This fourth volume of the landmark handbook focuses on the design, testing, and thermal management of 3D-integrated circuits, both from a technological and materials science perspective. Edited and authored by key contributors from top research institutions and high-tech companies, the first part of the book provides an overview of the latest developments in 3D chip design, including challenges and opportunities. The second part focuses on the test methods used to assess the quality and reliability of the 3D-integrated circuits, while the third and final part deals with thermal management and advanced cooling technologies and their integration.

ELECTRONIC DESIGN

MATERIALS FOR ADVANCED PACKAGING

Springer Significant progress has been made in advanced packaging in recent years. Several new packaging techniques have been developed and new packaging materials have been introduced. This book provides a comprehensive overview of the recent developments in this industry, particularly in the areas of microelectronics, optoelectronics, digital health, and bio-medical applications. The book discusses established techniques, as well as emerging technologies, in order to provide readers with the most up-to-date developments in advanced packaging.

ADVANCES IN EMBEDDED AND FAN-OUT WAFER LEVEL PACKAGING TECHNOLOGIES

Wiley-IEEE Press Examines the advantages of Embedded and FO-WLP technologies, potential application spaces, package structures available in the industry, process flows, and material challenges Embedded and fan-out wafer level packaging (FO-WLP) technologies have been developed across the industry over the past 15 years and have been in high volume manufacturing for nearly a decade. This book covers the advances that have been made in this new packaging technology and discusses the many benefits it provides to the electronic packaging industry and supply chain. It provides a compact overview of the major types of technologies offered in this field, on what is available, how it is processed, what is driving its development, and the pros and cons. Filled with contributions from some of the field’s leading experts, Advances in Embedded and Fan-Out Wafer Level Packaging Technologies begins with a look at the history of the technology. It then goes on to examine the biggest technology and marketing trends. Other sections are dedicated to chip-first FO-WLP, chip-last FO-WLP, embedded die packaging, materials challenges, equipment challenges, and resulting technology fusions. Discusses specific company standards and their development results Content relates to practice as well as to contemporary and future challenges in electronics system integration and packaging Advances in Embedded and Fan-Out Wafer Level Packaging Technologies will appeal to microelectronic packaging engineers, managers, and decision makers working in OEMs, IDMs, IFMs, OSATs, silicon foundries, materials suppliers, equipment suppliers, and CAD tool suppliers. It is also an excellent book for professors and graduate students working in microelectronic packaging research.

HETEROGENEOUS INTEGRATIONS

Springer

FAN-OUT WAFER-LEVEL PACKAGING

Springer This comprehensive guide to fan-out wafer-level packaging (FOWLP) technology compares FOWLP with flip chip and fan-in wafer-level packaging. It presents the current knowledge on these key enabling technologies for FOWLP, and discusses several packaging technologies for future trends. The Taiwan Semiconductor Manufacturing Company (TSMC) employed their InFO (integrated fan-out) technology in A10, the application processor for Apple’s iPhone, in 2016, generating great excitement about FOWLP technology throughout the semiconductor packaging community. For many practicing engineers and managers, as well as scientists and researchers, essential details of FOWLP – such as the temporary bonding and de-bonding of the carrier on a reconstituted wafer/panel, epoxy molding

compound (EMC) dispensing, compression molding, Cu revealing, RDL fabrication, solder ball mounting, etc. – are not well understood. Intended to help readers learn the basics of problem-solving methods and understand the trade-offs inherent in making system-level decisions quickly, this book serves as a valuable reference guide for all those faced with the challenging problems created by the ever-increasing interest in FOWLP, helps to remove roadblocks, and accelerates the design, materials, process, and manufacturing development of key enabling technologies for FOWLP.

ELECTROMAGNETIC COMPATIBILITY OF INTEGRATED CIRCUITS

TECHNIQUES FOR LOW EMISSION AND SUSCEPTIBILITY

Springer Science & Business Media Electromagnetic Compatibility of Integrated Circuits: Techniques for Low Emission and Susceptibility focuses on the electromagnetic compatibility of integrated circuits. The basic concepts, theory, and an extensive historical review of integrated circuit emission and susceptibility are provided. Standardized measurement methods are detailed through various case studies. EMC models for the core, I/Os, supply network, and packaging are described with applications to conducted switching noise, signal integrity, near-field and radiated noise. Case studies from different companies and research laboratories are presented with in-depth descriptions of the ICs, test set-ups, and comparisons between measurements and simulations. Specific guidelines for achieving low emission and susceptibility derived from the experience of EMC experts are presented.

INTEGRATED CIRCUIT PACKAGING, ASSEMBLY AND INTERCONNECTIONS

Springer Science & Business Media Reviewing the various IC packaging, assembly, and interconnection technologies, this professional reference provides an overview of the materials and the processes, as well as the trends and available options that encompass electronic manufacturing. It covers both the technical issues and touches on some of the reliability concerns with the various technologies applicable to packaging and assembly of the IC. The book discusses the various packaging approaches, assembly options, and essential manufacturing technologies, among other relevant topics.

THREE-DIMENSIONAL INTEGRATION AND MODELING

A REVOLUTION IN RF AND WIRELESS PACKAGING

Morgan & Claypool Publishers This book presents a step-by-step discussion of the 3D integration approach for the development of compact system-on-package (SOP) front-ends.Various examples of fully-integrated passive building blocks (cavity/microstip filters, duplexers, antennas), as well as a multilayer ceramic (LTCC) V-band transceiver front-end midule demonstrate the revolutionary effects of this approach in RF/Wireless packaging and multifunctional miniaturization. Designs covered are based on novel ideas and are presented for the first time for millimeterwave (60GHz) ultrabroadband wireless modules. Table of Contents: Introduction / Background on Technologies for Millimeter-Wave Passive Front-Ends / Three-Dimensional Packaging in Multilayer Organic Substrates / Microstrip-Type Integrated Passives / Cavity-Type Integrated Passives / Three-Dimensional Antenna Architectures / Fully Integrated Three-Dimensional Passive Front-Ends / References

DESIGN AND MODELING FOR 3D ICS AND INTERPOSERS

World Scientific 3D Integration is being touted as the next semiconductor revolution. This book provides a comprehensive coverage on the design and modeling aspects of 3D integration, in particularly, focus on its electrical behavior. Looking from the perspective the Silicon Via (TSV) and Glass Via (TGV) technology, the book introduces 3DICs and Interposers as a technology, and presents its application in numerical modeling, signal integrity, power integrity and thermal integrity. The authors underscored the potential of this technology in design exchange formats and power distribution.

MATERIALS AND TECHNOLOGIES FOR 3-D INTEGRATION

SYMPOSIUM HELD DECEMBER 1-3, 2008, BOSTON, MASSACHUSETTS, U.S.A.

THREE-DIMENSIONAL INTEGRATED CIRCUIT DESIGN

Morgan Kaufmann With vastly increased complexity and functionality in the "nanometer era" (i.e. hundreds of millions of transistors on one chip), increasing the performance of integrated circuits has become a challenging task. Connecting effectively (interconnect design) all of these chip elements has become the greatest determining factor in overall performance. 3-D integrated circuit design may offer the best solutions in the near future. This is the first book on 3-D integrated circuit design, covering all of the technological and design aspects of this emerging design paradigm, while proposing

effective solutions to specific challenging problems concerning the design of 3-D integrated circuits. A handy, comprehensive reference or a practical design guide, this book provides a sound foundation for the design of 3-D integrated circuits. * Demonstrates how to overcome "interconnect bottleneck" with 3-D integrated circuit design...leading edge design techniques offer solutions to problems (performance/power consumption/price) faced by all circuit designers * The FIRST book on 3-D integrated circuit design...provides up-to-date information that is otherwise difficult to find * Focuses on design issues key to the product development cycle...good design plays a major role in exploiting the implementation flexibilities offered in the 3-D * Provides broad coverage of 3-D integrated circuit design, including interconnect prediction models, thermal management techniques, and timing optimization...offers practical view of designing 3-D circuits

WIRELESS INTERFACE TECHNOLOGIES FOR 3D IC AND MODULE INTEGRATION

Cambridge University Press Synthesising fifteen years of research, this authoritative text provides a comprehensive treatment of two major technologies for wireless chip and module interface design, covering technology fundamentals, design considerations and tradeoffs, practical implementation considerations, and discussion of practical applications in neural network, reconfigurable processors, and stacked SRAM. It explains the design principles and applications of two near-field wireless interface technologies for 2.5-3D IC and module integration respectively, and describes system-level performance benefits, making this an essential resource for researchers, professional engineers and graduate students performing research in next-generation wireless chip and module interface design.

MORE-THAN-MOORE 2.5D AND 3D SIP INTEGRATION

Springer This book presents a realistic and a holistic review of the microelectronic and semiconductor technology options in the post Moore’s Law regime. Technical tradeoffs, from architecture down to manufacturing processes, associated with the 2.5D and 3D integration technologies, as well as the business and product management considerations encountered when faced by disruptive technology options, are presented. Coverage includes a discussion of Integrated Device Manufacturer (IDM) vs Fabless, vs Foundry, and Outsourced Assembly and Test (OSAT) barriers to implementation of disruptive technology options. This book is a must-read for any IC product team that is considering getting off the Moore’s Law track, and leveraging some of the More-than-Moore technology options for their next microelectronic product.

WAFER-LEVEL CHIP-SCALE PACKAGING

ANALOG AND POWER SEMICONDUCTOR APPLICATIONS

Springer Analog and Power Wafer Level Chip Scale Packaging presents a state-of-art and in-depth overview in analog and power WLCSP design, material characterization, reliability and modeling. Recent advances in analog and power electronic WLCSP packaging are presented based on the development of analog technology and power device integration. The book covers in detail how advances in semiconductor content, analog and power advanced WLCSP design, assembly, materials and reliability have co-enabled significant advances in fan-in and fan-out with redistributed layer (RDL) of analog and power device capability during recent years. Since the analog and power electronic wafer level packaging is different from regular digital and memory IC package, this book will systematically introduce the typical analog and power electronic wafer level packaging design, assembly process, materials, reliability and failure analysis, and material selection. Along with new analog and power WLCSP development, the role of modeling is a key to assure successful package design. An overview of the analog and power WLCSP modeling and typical thermal, electrical and stress modeling methodologies is also presented in the book.

NANOMETER CMOS ICS

FROM BASICS TO ASICS

Springer This textbook provides a comprehensive, fully-updated introduction to the essentials of nanometer CMOS integrated circuits. It includes aspects of scaling to even beyond 12nm CMOS technologies and designs. It clearly describes the fundamental CMOS operating principles and presents substantial insight into the various aspects of design implementation and application. Coverage includes all associated disciplines of nanometer CMOS ICs, including physics, lithography, technology, design, memories, VLSI, power consumption, variability, reliability and signal integrity, testing, yield, failure analysis, packaging, scaling trends and road blocks. The text is based upon in-house Philips, NXP Semiconductors, Applied Materials, ASML, IMEC, ST-Ericsson, TSMC, etc., courseware, which, to date, has been completed by more than 4500 engineers working in a large variety of related disciplines: architecture, design, test, fabrication process, packaging, failure analysis and software.

MATHEMATICS FOR MACHINE LEARNING

Cambridge University Press Distills key concepts from linear algebra, geometry, matrices, calculus, optimization, probability and statistics that are used in machine learning.

BIO AND NANO PACKAGING TECHNIQUES FOR ELECTRON DEVICES

ADVANCES IN ELECTRONIC DEVICE PACKAGING

Springer Science & Business Media This book discusses future trends and developments in electron device packaging and the opportunities of nano and bio techniques as future solutions. It describes the effect of nano-sized particles and cell-based approaches for packaging solutions with their diverse requirements. It offers a comprehensive overview of nano particles and nano composites and their application as packaging functions in electron devices. The importance and challenges of three-dimensional design and computer modeling in nano packaging is discussed; also ways for implementation are described. Solutions for unconventional packaging solutions for metallizations and functionalized surfaces as well as new packaging technologies with high potential for industrial applications are discussed. The book brings together a comprehensive overview of nano scale components and systems comprising electronic, mechanical and optical structures and serves as important reference for industrial and academic researchers.

ANTENNA-IN-PACKAGE TECHNOLOGY AND APPLICATIONS

John Wiley & Sons A comprehensive guide to antenna design, manufacturing processes, antenna integration, and packaging Antenna-in-Package Technology and Applications contains an introduction to the history of AiP technology. It explores antennas and packages, thermal analysis and design, as well as measurement setups and methods for AiP technology. The authors—well-known experts on the topic—explain why microstrip patch antennas are the most popular and describe the myriad constraints of packaging, such as electrical performance, thermo-mechanical reliability, compactness, manufacturability, and cost. The book includes information on how the choice of interconnects is governed by JEDEC for automatic assembly and describes low-temperature co-fired ceramic, high-density interconnects, fan-out wafer level packaging–based AiP, and 3D-printing-based AiP. The book includes a detailed discussion of the surface laminar circuit–based AiP designs for large-scale mm-wave phased arrays for 94-GHz imagers and 28-GHz 5G New Radios. Additionally, the book includes information on 3D AiP for sensor nodes, near-field wireless power transfer, and IoT applications. This important book: • Includes a brief history of antenna-in-package technology • Describes package structures widely used in AiP, such as ball grid array (BGA) and quad flat no-leads (QFN) • Explores the concepts, materials and processes, designs, and verifications with special consideration for excellent electrical, mechanical, and thermal performance Written for students in electrical engineering, professors, researchers, and RF engineers, Antenna-in-Package Technology and Applications offers a guide to material selection for antennas and packages, antenna design with manufacturing processes and packaging constraints, antenna integration, and packaging.